A Unidirectional Snubber Less Fully Soft-switched Single Stage Three Phase High Frequency Link DC/AC Converter

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***Abstract*—In this paper, a high frequency link, single stage, three phase DC-AC converter topology is proposed. The converter is suitable for applications like grid integration of photovoltaic, fuel cell where power flow is mainly unidirectional. The DC side of the converter is fully soft-switched (zero voltage switched). The AC side of the converter is line frequency switched. The use of high frequency transformer (HFT) helps to achieve high power density by reducing the size of the magnetics. A small shunt compensator is used at the grid end to ensure the unity power factor operation of the converter. A detail analysis of the converter operation is discussed in this paper. Important simulation results verifying the converter operation are also presented.**

Index Terms- Single stage DC-AC converter, modulation technique, high-frequency-link, soft-switching, line frequency switching

I. Introduction

Present global warming scenario is giving fresh impetus to the grid integration of renewable energy sources to reduce the dependence on fossil fuel. Conventionally, grid tied inverters with line frequency transformer (LFT) [1] are used at the grid interface. These LFTs provide required voltage magnification, galvanic isolation as well as reduce leakage current in the system. But the bulky LFTs increase the overall volume and cost of the system. An alternative approach is to use high frequency transformer (HFT) based inverter topologies for grid integration. The HFTs reduces the volume, weight and cost of the system by reducing the size of the magnetics [2]. The HFT based DC-AC converters are either multi-stage [3] type where a isolated DC-DC stage is cascaded with a DC- line frequency AC stage through a bulky DC link capacitor or single stage type where no DC link filter capacitor is used in-between stages. In case of a single stage topology, the output of the HFT is either rectified and then inverted to produce line frequency AC [4] by a synchronous rectifier and 3ϕ VSI stage or a cyclo-converter [5] is used to directly converter the high frequency AC to required magnitude line frequency AC. In literature different modulation strategy is employed to achieve soft switching of HF link converter. Additional snubber circuits are used to commute the leakage energy of the HFT. The commutation of leakage energy without additional snubber circuits are shown in [6], [7]. The converter switching loss can be improved further if the converter is switched at high frequency only for some portion of the line frequency cycle. In [8], [9] the modulation strategies are such that the AC side converter is HF switched only for one third of the line frequency cycle.

In this paper a single stage, three phase, HFL DC-AC converter topology (see Fig. 1) is reported. The proposed topology can be used for the applications like grid integration of photovoltaic or fuel cell where power flow is mainly unidirectional. The converter topology with the proposed modulation scheme has following features: (a) single stage unidirectional (DC-AC) power conversion, (b) the DC side high frequency converter is fully soft-switched, (c) commutation of leakage energy of HFT without additional snubber circuits, (d) the AC side converter switches are line frequency switched incurring negligible switching losses. So, the AC side converter can be implemented using high voltage blocking inherently slow semiconductor switches for medium voltage grid integration, (e) use of HFT reduces volume and cost of the system, (f) a 4.5% rated shunt compensator at the grid end ensures the unity power factor (UPF) operation of the converter.

The paper is organised as follows. In section II, the modulation strategy and soft-switching technique are described in details. Reactive compensation scheme is described in section III. In section IV, important simulation results are presented to validate the converter operation.

II. Steady state operation

This section describes steady state operation of the converter in details. At first, the modulation strategy describing the generation of 3ϕ balanced output voltage is discussed. Then the soft-switching process of the primary side high frequency inverter is described.

A. Modulation scheme

The primary side high frequency inverter is pulse width modulated to generate balanced 3ϕ line frequency AC voltage at the grid end. The 3ϕ modulation signals $d_{a,b,c}(t)$ and saw-tooth carrier are shown in Fig. 2. These modulation signals are in same phase with their respective line currents $i_{a,b,c}$. The primary side HF inverter has four legs. The leg with switch pair $S_{1,2}$ are complementary switched at half of the carrier frequency $\frac{1}{T_S}$ with 50% duty ratio (see Fig. 3a). The strategies used to generate the gating signals

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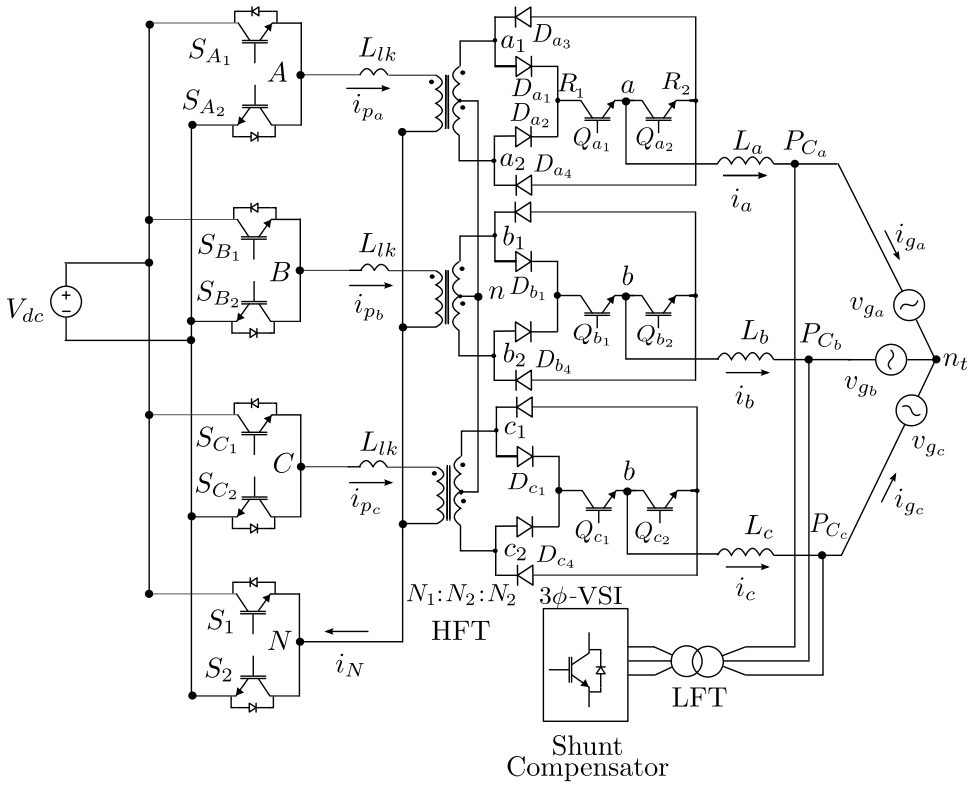


Fig. 1: Circuit diagram of the proposed 3ϕ DC/AC converter.

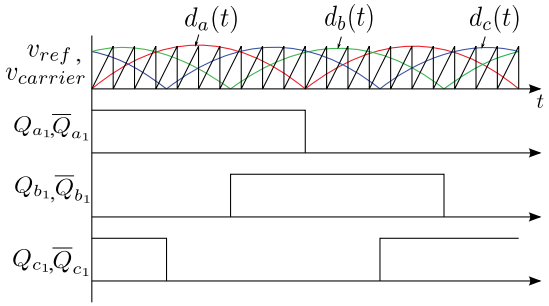
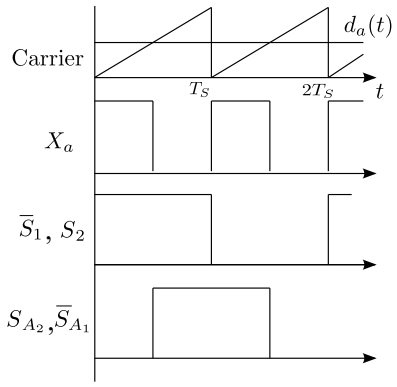
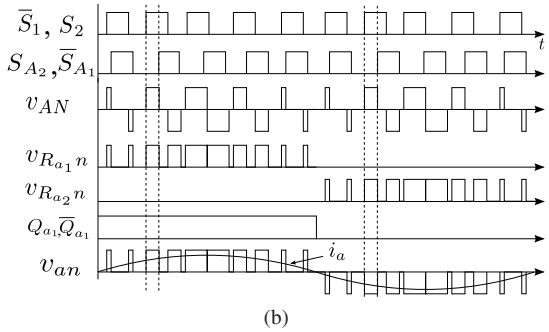


Fig. 2: 3ϕ modulation signals with sawtooth carrier and the gating signals of secondary side line frequency switches.



(a)



(b)

Fig. 3: (a) Control signals generating gating signals of HF inverter, (b) overall modulation scheme showing generation of phase a voltage.

are similar for three legs corresponding to three phases. Here the scheme describing generation of gating signals of S_{A_1,A_2} corresponding to phase a is discussed in details and is shown in Fig. 3. The modulation signal corresponding to phase a is given as-

$$d_a(t) = M|\sin(2\pi ft)| \tag{1}$$

where M is peak modulation index and f is grid frequency. $d_a(t)$ is compared with unipolar sawtooth carrier to generate a control signal X_a. $X_a(t)$ is defined as-

$$X_a(t) = \begin{cases} 1, & d_a(t) \geq Carrier(t) \\ 0, & otherwise \end{cases} \tag{2}$$

The gating signal of S_{A_1,A_2} are given as-

$$G_{S_{A_2}} = G_{S_2} \oplus X \tag{3}$$

$$G_{S_{A_1}} = \overline{G}_{S_{A_2}} \tag{4}$$

Above switching scheme generates pulse width modulated (PWM) high frequency ($\frac{1}{2T_S}$) square voltage pulses across the high frequency transformer (HFT) primary AN. This high frequency inversion ensures the transformer flux balance over one switching cycle ($2T_S$). The applied voltage v_{AN} as shown in Fig. 3b has three levels: $\pm V_{dc}$ and zero. Only non-zero states of v_{AN} are responsible for active power transfer. The secondary side diode bridge D_{a_1}-D_{a_4} with the switch pair Q_{a_1,a_2} rectifies the high frequency to generate line frequency PWM AC (v_{an}). The switches Q_{a_1,a_2} are turned on based on the direction of line current i_a. These switches are switched at line frequency as shown in Fig. 3b. The average PWM line frequency AC output can be expressed as-

$$\overline{v}_{an}(t) = T_r M \sin(2\pi f t) \tag{5}$$

where $T_r = \dfrac{N_2}{N_1}$, turns ratio of the HFT.

B. Soft-switching technique

The primary side three phase four leg high frequency inverter is fully soft switched. The soft-switching of the converter is achieved using device capacitance and leakage inductance of the HFT. The soft switching technique applied here is similar for all the three phases a, b and c. Only, the soft-switching process of phase a is described in details. The secondary side switches Q_{a_1,a_2}, Q_{b_1,b_2} and Q_{c_1,c_2} are line frequency switched based on the direction of line currents $i_{a,b,c}$. Hence switching loss of these switches are negligible. Q_{a_1,b_1,c_1} are ON when line currents are positive. The soft switching process is described here for positive line current i_a. For negative line current it follows the same sequence of operation. Properly filtered, slowly varying line current, i_a is considered to be constant in a high frequency switching cycle ($\frac{1}{2T_S}$). The switching process described here shows the polarity reversal of primary transformer current (i_{P_a}) from positive to negative in one half of the high frequency switching cycle. The same sequence is followed in the other half of the high frequency switching cycle with other symmetrical switches. Device switching waveforms and soft-switching process are shown in Fig. 4 and Fig.5 respectively. What follows is a detail description of the soft switching process of the proposed topology.

1) Mode I: (Fig. 5a, $t < t_0$): In this interval S_{A_1}, S_2 are ON and S_{A_1} is conducting the steady state primary current $i_{P_a} = T_r|i_a|$. The current through S_2 is given as $i_N = T_r(|i_a| + |i_b| + |i_c|)$. The direction of the primary current is considered as positive. In secondary, the diode D_{a_1} and the switch Q_{a_1} are conducting the line current i_a. The switching state applies a positive voltage V_{dc} across the transformer primary AN. During this interval active power flows from DC to AC side of the converter. The devices S_{A_2} and S_1 block V_{dc} voltage.

2) Mode II: (Fig. 5b, $t_0 < t < t_1$): At $t = t_0$, S_{A_1} is turned OFF. Considering the device capacitance, the voltage across S_{A_1} can not rise immediately after the turn OFF. So, S_{A_1} is zero voltage turn OFF. The primary current i_{P_a} starts charging the device capacitance (C_{A_1}) of S_{A_1} and

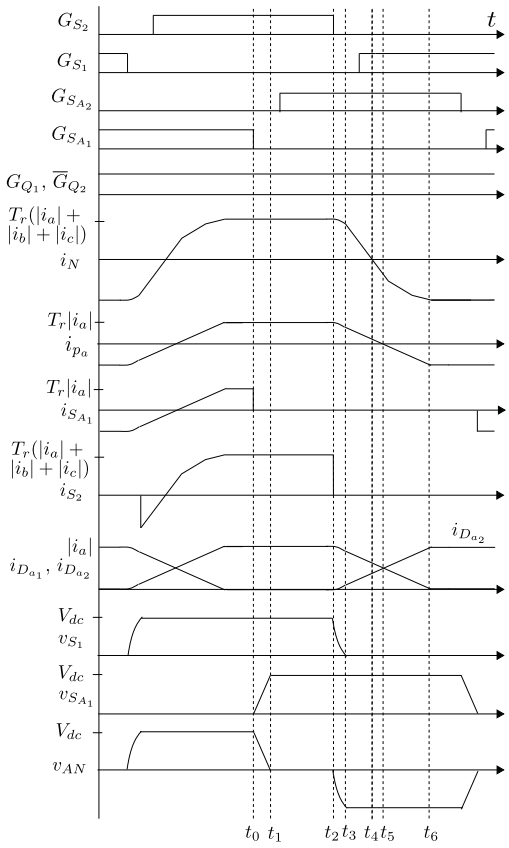


Fig. 4: Device voltage and current waveforms during commutation process.

discharging C_{A_2}, the device capacitance of S_{A_2}. i_{P_a} and i_N remain same as in Mode I. The circuit equations are-

$$v_{C_{A_1}} + v_{C_{A_2}} = V_{dc} \tag{6}$$

$$C_{A_2}\frac{dv_{C_{A_2}}}{dt} = C_{A_1}\frac{dv_{C_{A_1}}}{dt} + i_{P_a} \tag{7}$$

Solving (6) and (7), voltage across S_{A_2} is given as-

$$v_{C_{A_2}}(t) = V_{dc} - \frac{T_r i_a}{C_{A_1} + C_{A_2}}t \tag{8}$$

At t_1, C_{A_2} discharges completely and $v_{C_{A_2}}$ can not be negative as the body diode of S_{A_2} is forward biased.

3) Mode III: (Fig. 5c, $t_1 < t < t_2$): In this interval the primary current i_{P_a} circulates through the body diode of S_{A_2} and the switch S_2. To achieve zero voltage (ZV) turn ON of S_{A_2}, the gating pulse is applied. This switching state applies zero voltage across the transformer primary AN. This interval is a zero state as there is no active power flow. The secondary side line current i_a free-wheels through D_{a_1} and Q_{a_1}.

4) Mode IV: (Fig. 5d, $t_2 < t < t_3$): At t_2, the switch S_2 is turned OFF. This is again a capacitor assisted zero voltage type soft turn OFF. The neutral current i_N starts charging the device capacitance (C_2) of S_2 and discharging C_1 of S_1. This applies a negative voltage across the transformer primary AN which forward-biases secondary

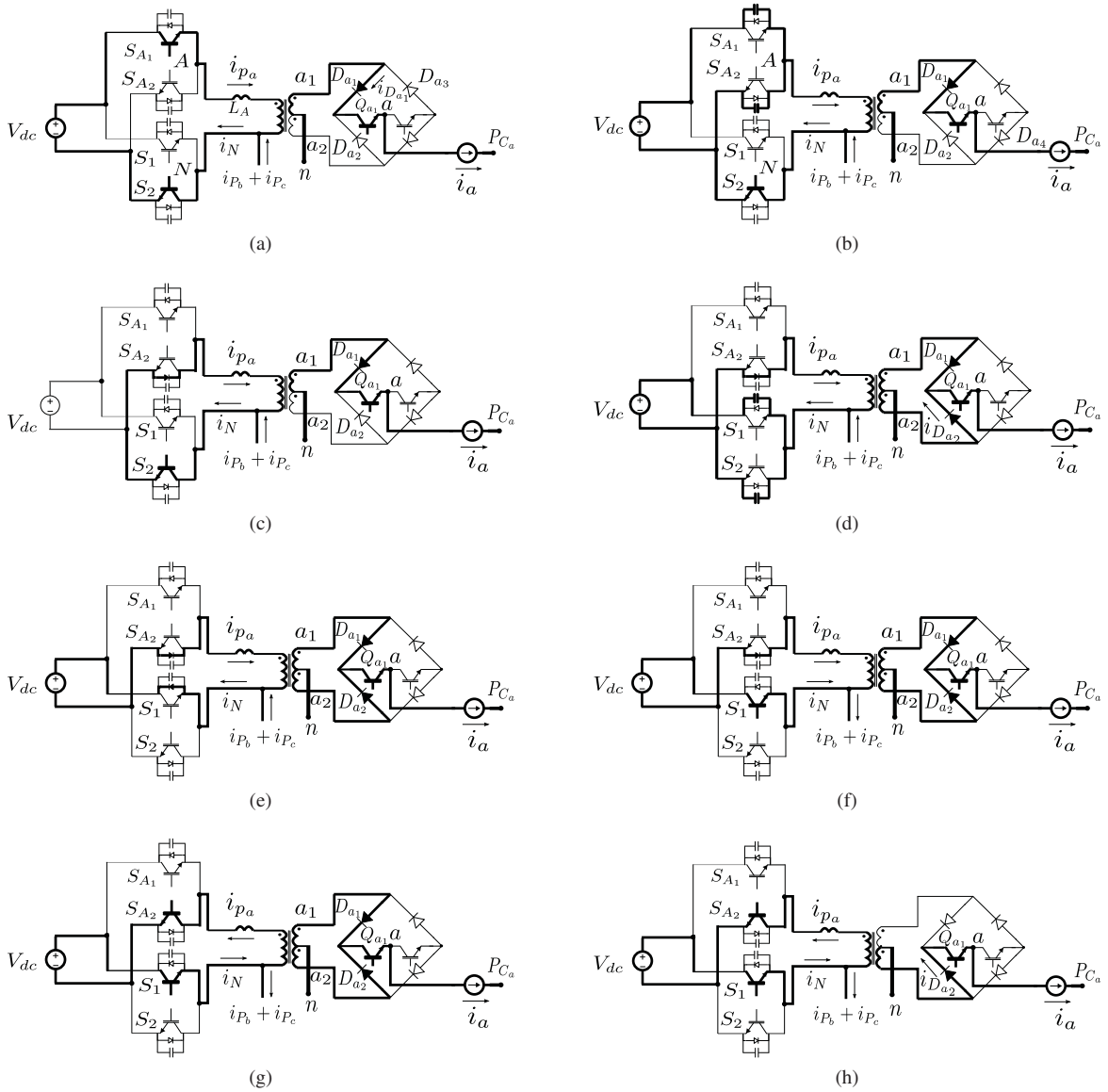


Fig. 5: Commutation process- (a) $t < t_0$, (b) $t_0 < t < t_1$, (c) $t_1 < t < t_2$, (d) $t_2 < t < t_3$, (e) $t_3 < t < t_4$, (f) $t_4 < t < t_5$, (g) $t_5 < t < t_6$, (h) $t > t_6$.

side diode D_{a_2}. The primary currents start falling during this interval. As the neutral current i_N consists of phase currents $i_{P_{a,b,c}}$, any change in the phase currents is reflected on i_N. Additional figures showing commutation process of $i_{P_{b,c}}$ with i_{P_a} are presented in Fig. 7 and the phase current waveforms are given in Fig. 6. In Fig. 7, following colour code is used: red indicates circuit is in steady state and the branch current is constant, whereas black indicates the circuit is going through a transient condition. The circuit equations are given as-

$$i_{D_{a_1}} + i_{D_{a_2}} = i_a \tag{9}$$

$$i_{P_a} = T_r(i_{D_{a_1}} - i_{D_{a_2}}) \tag{10}$$

$$i_N = i_{P_a} + i_{P_b} + i_{P_c} \tag{11}$$

$$C_2 \frac{dv_{C_2}}{dt} = C_1 \frac{dv_{C_1}}{dt} + i_N \tag{12}$$

$$v_{C_2} + v_{C_1} = V_{dc} \tag{13}$$

$$v_{C_2} + \frac{L_{lk}}{3}\left(\frac{di_N}{dt}\right) = 0 \tag{14}$$

where L_{lk} leakage inductance of HFT.

$$\frac{di_{P_a}}{dt} = \frac{di_{P_b}}{dt} = \frac{di_{P_c}}{dt} = -\frac{v_{C_2}}{L_{lk}} \tag{15}$$

Solving equations (9)-(15), following expressions are given as-

$$i_N(t) = i_N(t_2)\cos\left(\frac{\sqrt{3}t}{\sqrt{L_{lk}(C_1 + C_2)}}\right) \tag{16}$$

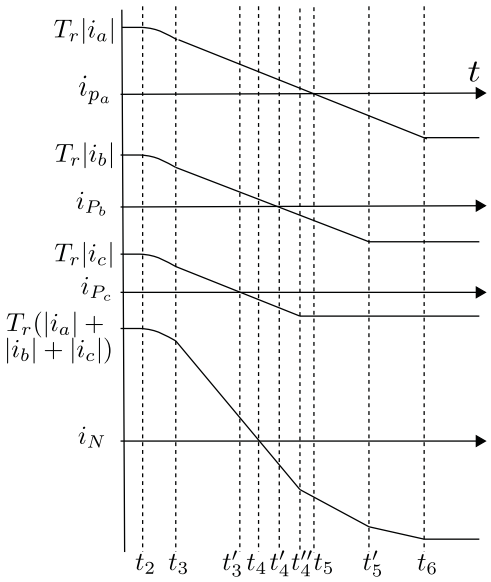


Fig. 6: Primary current waveforms during $t_2 < t < t_6$.

where $i_N(t_2) = T_r(|i_a| + |i_b| + |i_c|)$.

$$i_{P_a}(t) = i_{P_a}(t_2)\cos\left(\frac{t}{\sqrt{L_{lk}(C_1+C_2)}}\right) \tag{17}$$

where $i_{P_a}(t_2) = T_r|i_a|$. i_{P_b} and i_{P_c} have similar expressions. Secondary side diode currents are given as-

$$i_{D_{a_1}}(t) = \frac{i_a}{2}\left(1+\cos\frac{t}{\sqrt{L_{lk}(C_1+C_2)}}\right) \tag{18}$$

$$i_{D_{a_2}}(t) = \frac{i_a}{2}\left(1-\cos\frac{t}{\sqrt{L_{lk}(C_1+C_2)}}\right) \tag{19}$$

Voltage across the device S_1 is given as-

$$v_{C_1} = V_{dc} - i_N(t_2)\sqrt{\frac{L_{lk}}{3(C_1+C_2)}}\sin\left(\frac{\sqrt{3}t}{\sqrt{L_{lk}(C_1+C_2)}}\right) \tag{20}$$

At t_3, C_1 discharges to zero and the body diode of S_1 is forward biased. v_{C_2} reaches to blocking voltage V_{dc}.

5) Mode V: (Fig. 5e, $t_3 < t < t_4$): From this interval the following situation is considered to describe the switching process: $|i_a| > |i_b| > |i_c|$. For other situations the switching process remains same except the timings where $i_{P_{a,b,c}}$ are changing the direction and reaching steady state, are interchanged based on the magnitude of $i_{a,b,c}$. In this interval the body diodes of S_2 and switches S_{A_2,B_2,C_2} are conducting the primary currents $i_{P_{a,b,c}}$ and a negative voltage $-V_{dc}$ is applied across the transformer primaries (see Fig. 7c). The circuit equations are-

$$V_{dc} + \frac{L_{lk}}{3}\frac{di_N}{dt} = 0 \tag{21}$$

$$V_{dc} + L_{lk}\frac{di_{P_{a,b,c}}}{dt} = 0 \tag{22}$$

solving equations (21) and (22) the primary currents are expressed as-

$$i_N(t) = i_N(t_3) - \frac{3V_{dc}}{L_{lk}}(t-t_3) \tag{23}$$

$$i_{P_{a,b,c}}(t) = i_{P_{a,b,c}}(t_3) - \frac{V_{dc}}{L_{lk}}(t-t_3) \tag{24}$$

The secondary side diode currents are given as-

$$i_{D_{a_1}}(t) = \frac{i_a}{2} + \frac{i_{P_a}(t_3)}{2T_r} - \frac{V_{dc}}{2T_rL_{lk}}(t-t_3) \tag{25}$$

$$i_{D_{a_2}}(t) = \frac{i_a}{2} - \frac{i_{P_a}(t_3)}{2T_r} + \frac{V_{dc}}{2T_rL_{lk}}(t-t_3) \tag{26}$$

At $t = t_3'$, i_{P_c} becomes zero and continues to fall with same slope (see Fig. 6). After t_3', i_{P_c} is negative and flows through the switch S_{C_2} (see Fig. 7d). At $t = t_4$, i_N reaches zero and then becomes negative. To achieve ZVS turn on of S_1 following conditions are to be satisfied:

$$(|i_a| + |i_b| + |i_c|) > \frac{V_{dc}}{T_r}\sqrt{\frac{3(C_1+C_2)}{L_{lk}}} \tag{27}$$

$$(t_3 - t_2) < DT < (t_4 - t_2) \tag{28}$$

where DT is the dead time between S_1 and S_2.

6) Mode VI: (Fig. 5f, $t_4 < t < t_5$): As i_N becomes negative after t_4, the switch S_1 starts conducting (see Fig. 7e). $i_{P_{a,b,c}}$, $i_{D_{a_1}}$ and i_N continue to fall with same slope as in mode V (see Fig. 6). At $t = t_4'$, i_{P_b} reaches zero and then becomes negative. S_{B_2} starts conducting i_{P_b} (see Fig. 7f). At t_4'', i_{P_c} reaches the negative steady state value $-T_r|i_c|$ (see Fig. 6) and the branch carrying i_{P_c} is marked in red (see Fig. 7g) to indicate steady state condition. The slope of the neutral current has changed and i_N can be expressed as-

$$i_N(t) = i_N(t_4'') - \frac{2V_{dc}}{L_{lk}}(t-t_4'') \tag{29}$$

At $t = t_5$, primary current i_{P_a} reaches zero and then becomes negative. The switch S_{A_2} starts conducting i_{P_a} (see Fig. 7h). The secondary side currents $i_{D_{a_1}} = i_{D_{a_2}} = \frac{i_a}{2}$

7) Mode VII: (Fig. 5g, $t_5 < t < t_6$): In this interval i_N, $i_{P_{a,b}}$ and $i_{D_{a_1}}$ keep on falling with same slope as in last interval. At t_5' i_{P_b} reaches to steady state value $-T_r|i_b|$ (see Fig. 7i and 6). The slope of i_N has changed again.

$$i_N(t) = i_N(t_5') - \frac{V_{dc}}{L_{lk}}(t-t_5') \tag{30}$$

At $t = t_5$, i_{P_a} and i_N reach to steady state value $-T_r|i_a|$ and $-T_r(|i_a| + |i_b| + |i_c|)$ respectively. In secondary side, $i_{D_{a_1}}$ reaches zero and D_{a_2} takes full current i_a.

8) Mode VIII: (Fig. 5h, $t > t_6$): In primary side, S_{A_2} , S_1 and in secondary side D_{a_2} , Q_{a_1} are conducting. This switching state applies a negative voltage across the transformer primary AN and the transformer primary current polarity is also negative. This is a similar switching state like Mode I where active power transfer is happening from DC to AC side.

The above discussion shows the current transfer from S_{A_1}, S_2, D_{a_1} to S_{A_2}, S_1, D_{a_2} as well as polarity reversal of the transformer primary current.

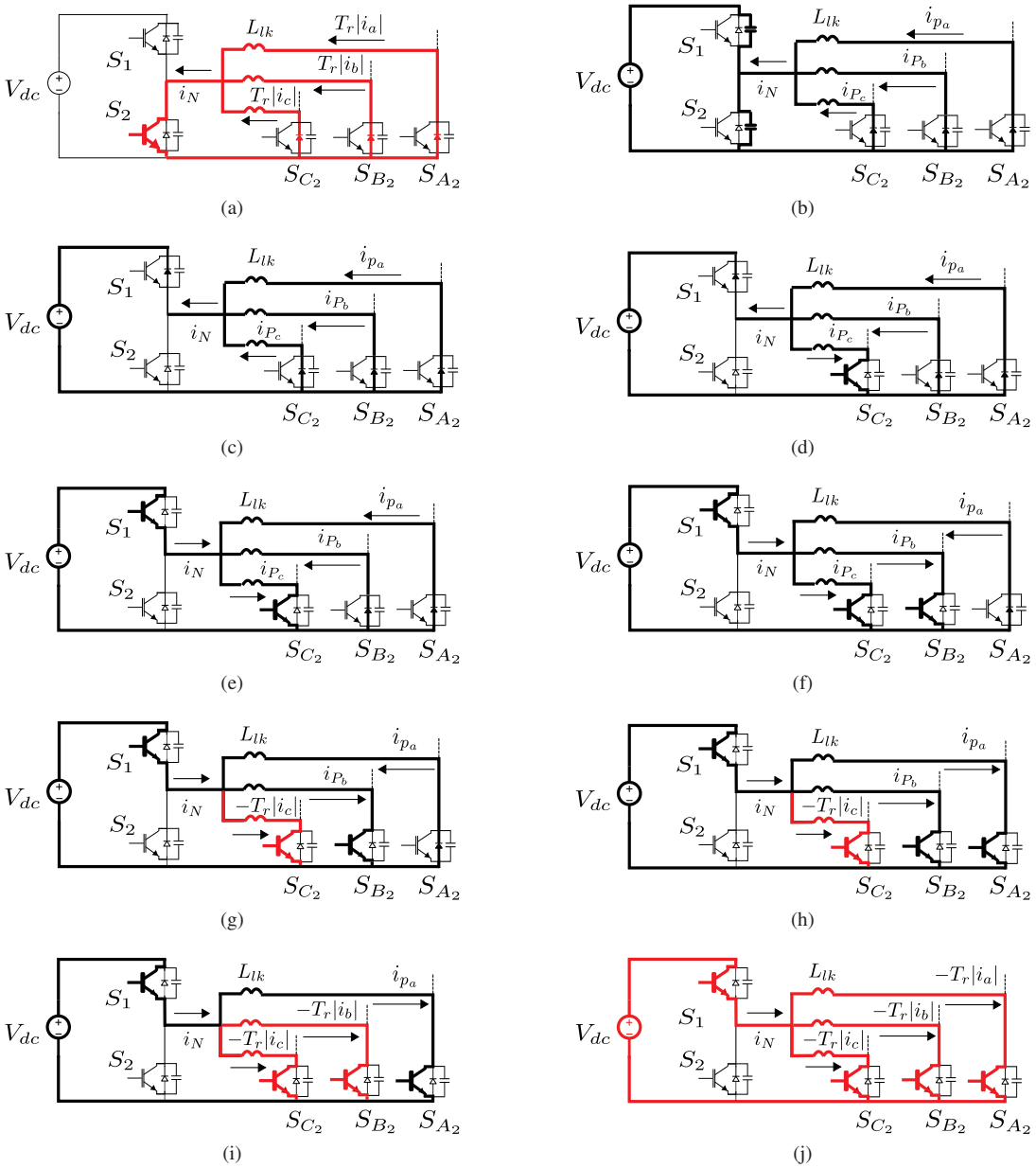


Fig. 7: Primary current commutation process in details- (a) $t < t_2$, (b) $t_2 < t < t_3$, (c) $t_3 < t < t_3'$, (d) $t_3' < t < t_4$, (e) $t_4 < t < t_4'$, (f) $t_4' < t < t_4''$, (g) $t_4'' < t < t_5$, (h) $t_5 < t < t_5'$, (i) $t_5' < t < t_6$, (j) $t > t_6$.

III. Reactive Compensation

The power flow of the proposed topology is unidirectional and the modulation strategy ensures unity power factor (UPF) operation of the converter. So, to meet the reactive power demand by the line and filter inductance at the grid interface a shunt compensator (3ϕ VSI) is used as shown in Fig. 1. What follows is the estimation of the power rating of the shunt compensator. The active power demand by the grid is given as-

$$P_a = 3|\overline{v}_{g_a}||\overline{i}_{g_a}| \tag{31}$$

Where, $\overline{v}_{g_a}$,$\overline{i}_{g_a}$ are r.m.s phase voltage and current at the grid end. Active power supplied by the converter is-

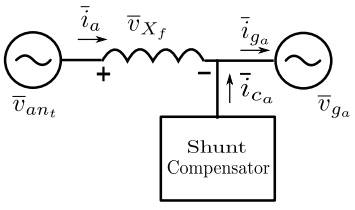
$$3|\overline{v}_{an_t}||\overline{i}_a| = P_a \tag{32}$$

Where, $\overline{v}_{an_t}$,$\overline{i}_a$ are r.m.s voltage and current of the converter. The equivalent compensation scheme can be presented as in Fig. 8. Following circuit equations can be written from Fig. 8a-

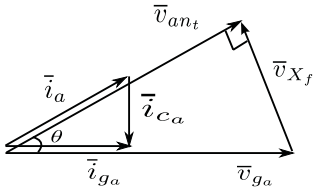
$$\overline{v}_{an_t} = \overline{v}_{g_a} + j \cdot X_f \cdot \overline{i}_a \tag{33}$$

$$\overline{i}_{g_a} = \overline{i}_a + \overline{i}_{c_a} \tag{34}$$

Where, $\overline{i}_{c_a}$ is the compensator current and X_f is the line reactance. Here $\overline{v}_{g_a} = 1$ p.u., $\overline{i}_{g_a} = 1$ p.u. and reactive



(a)



(b)

Fig. 8: Reactive power compensation: (a) scheme, (b) phasor diagram

drop $\bar{v}_{X_f} = 0.05$ p.u. is considered. Solving equations (31)-(34) following quantities are estimated- $\bar{v}_{an_t} = 0.9987$ p.u., $\bar{i}_a = 1.001$ p.u. and $\bar{i}_{c_a} = 0.045$ p.u. So, the reactive power supplied by the shunt compensator- $Q_{sh} = 3\bar{v}_{g_a}\bar{i}_{c_a} = 0.135$ p.u $\simeq 4.5\%$ of total power rating of the converter.

IV. Simulation Results

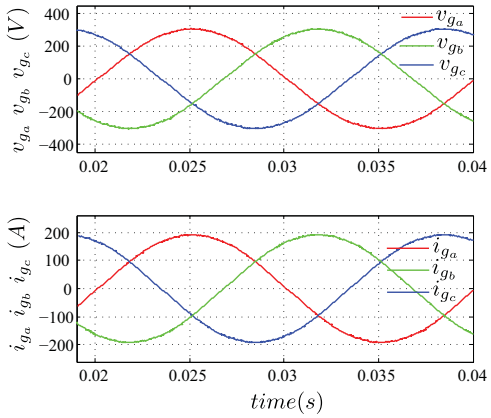
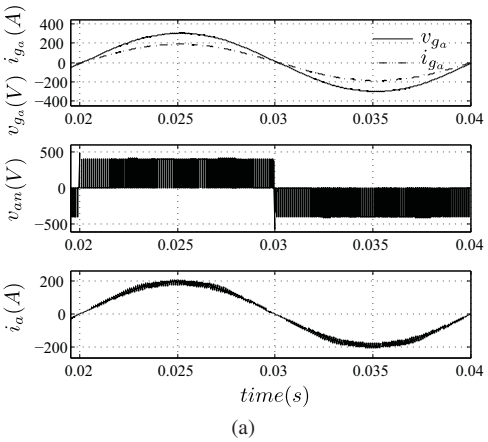


Fig. 9: Simulated 3ϕ output of the converter.

The proposed topology with the described modulation scheme is simulated in MATLAB simulink, supplying 100 kW power to the 400 V, 50 Hz grid. The DC link voltage used in the simulation is 600V. The DC side HF inverter is switched at 5 kHz. The leakage impedance of the HFT is considered to be 8.25μH (7.5 p.u.) and the device parasitic capacitances are 10 nF. The filter inductor used at the grid end is 0.25 mH. 1μs dead time is used in the simulation between any two complementary switches. The balanced 3ϕ grid voltage and current are shown in Fig. 9. The simulation result shows that the converter is supplying power to the grid at UPF. PWM pole voltage v_{aN} and phase current i_a before the filter stage is shown in Fig. 10a. Pulse width modulated input voltage v_{AN} of the HFT is shown in Fig. 10b. The HFT neutral current i_N and phase current i_{P_A}



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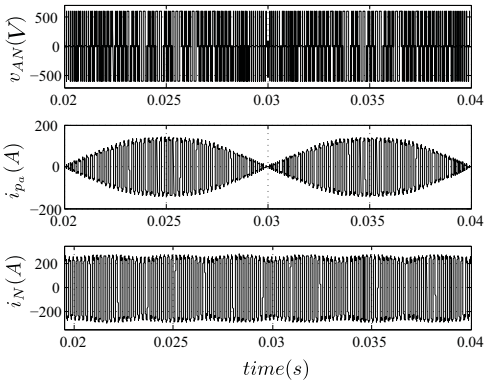
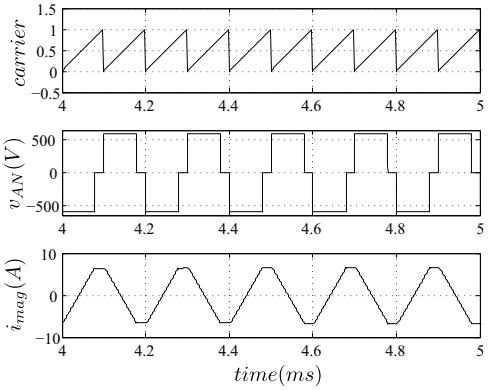
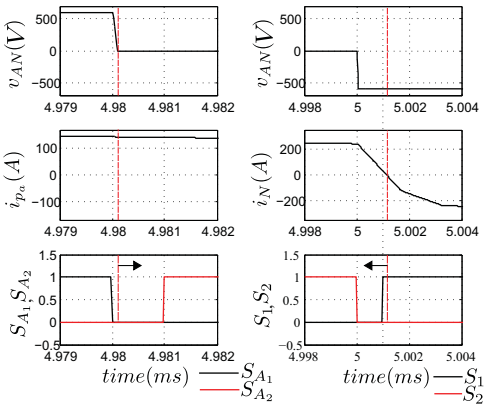


(b)



(c)



(d)

Fig. 10: Simulated waveforms of phase a - (a) pole voltage and current , (b) HFT voltage and current, (c) flux balance of HFT (c) ZVS-switching

are also presented in Fig. 10b. Unlike i_{P_a} the steady state magnitude of i_N never goes below 86.6% of the peak value. This helps to achieve soft-switching of $S_{1,2}$ even when i_{P_a} is zero. Fig. 10c shows the flux balance of the HFT over one switching cycle. The magnetising current i_{mag} does not contain any DC component. The soft-switching waveforms of the converter is shown in Fig. 10d. After turning OFF of S_{A_1}, gating pulse of S_{A_2} is applied only when body diode of S_{A_2} starts conducting and $v_{AN} = 0V$. The gating pulse of S_1 is applied before the current i_N becomes negative i.e when the body diode of S_1 is still conducting.

V. Conclusion

This paper demonstrate a modulation strategy and soft-switching technique of a novel single stage, high frequency link, three phase DC-AC converter topology. Following important features are discussed in this paper: i) the DC side HF inverter is fully zero voltage switched, ii) AC side converter is line frequency switched, iii) galvanic isolation between DC and AC side with high frequency transformer improves power density and cost of the system, iv) a small size voltage source inverter is used to compensate the reactive drop due to filter inductance. The steady state converter operation is discussed in details. The simulation results verify the converter operation. The proposed topology is suitable for medium voltage grid integration of renewable sources as high voltage blocking relatively slow semiconductor switches can be used in line frequency switched grid side converter.

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